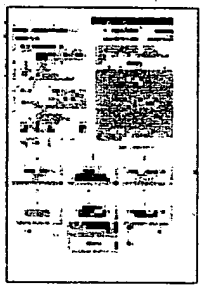
The Delphion Integrated View

Title: **JP62251949A2: ERROR CORRECTING METHOD FOR MEMORY DEVICE**

Country: **JP** Japan
Kind: **A**



View Image

1 page

Inventor: **OGASAWARA KOICHI;**

Assignee: **MITSUBISHI ELECTRIC CORP**
News, Profiles, Stocks and More about this company

Published / Filed: **1987-11-02** / 1986-04-25

Application Number: **JP1986000096332**

IPC Code: G06F 12/16;

Priority Number: 1986-04-25 **JP1986000096332**

Abstract: PURPOSE: To facilitate finding troubles of an error detecting circuit and a correcting circuit by checking again data after error correction to improve the reliability of a memory device.

CONSTITUTION: When an uncorrectable error is decided a detecting circuit 4 outputs the position of the error bit to an analyzing circuit 7 as a syndrome. The circuit 7 decides whether the error bit is within data or a check code, and the contents of a read data latch 2 are directly written in a read data buffer 6 if data bits have not the error. If data bits have the error, the bit indicated by the syndrome in data is corrected, and this corrected data is checked again by the contents of a check code latch 3. If there are no errors as the result of recheck, the processing is normally terminated; but other-wise, the processing is abnormally terminated.

INPADOC Legal Status: None **Get Now:** Family Legal Status Report

Family: Show 2 known family members

Other Abstract Info: None